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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/943,595	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,16,17 and 27-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,16,17 and 27-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-4, 16-17, and 27-54 has/have been presented for examination based on amendment filed on 24th January 2007.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26th December 2006 has been entered.
3. Claim(s) 1, 16, 27, 37, 39, 43, 45, 49 and 51 is/are amended.
4. Claim(s) 1 remain rejected under 35 USC § 101.
5. Claim(s) 1-4, 16-17, and 27-54 remain rejected under 35 USC § 103 under new grounds.
6. The arguments submitted by the applicant have been fully considered. Claims 1-4, 16-17, and 27-54 remain rejected and this action is made NON-FINAL. The examiner's response is as follows.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding Claim 1

Method claim 1 does not recite a tangible result to the preamble disclosing "exporting emulation information from the data processor" as the last step outputs the second sequence of second information blocks, but that information is not tangibly stored in any location once derived from the first information block. Hence, there is no indication there the results of outputting step are tangible. Applicant's attempt to cure the deficiency by "outputting said sequence of the second information blocks from the data processor integrated circuit to a host external to the data processor integrated circuit" still lacks tangibly storing the said second information.

Examiner suggests that the following modification (underlined) can overcome the deficiency cited above:

"outputting and storing said sequence of the second information blocks from the data processor integrated circuit to a host external to the data processor integrated circuit and stored on a host ".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 1-4, 16-17, 27,-29, 34, 37-39, 43-45, and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6,732,307 issued to Edwards further in view of U.S. Patent No. 5,848,264 issued to Baird et al.

Regarding Claim 1 (Updated)

Edwards teaches a method of exporting emulation information from a data processor *integrated circuit* (Edwards: Col. 2, Lines 31-33; *Col.1 Line 13-14 – SOC, 56-57-ICE*), comprising collecting internal emulation information from a data processor at a data processor clock rate (Edwards: Col. 2, Lines 12-19); arranging the collected emulation information into a plurality of first information blocks having a first fixed size (Edwards: Col. 17, Lines 45-52).

Edwards teaches receiving the plurality of first information blocks (Edwards: Col. 17, Lines 45-52 in trace buffer 227) and arranging (e.g. PC compression) the emulation information contained therein into a plurality of second information blocks (Edwards: having a second fixed size which differs from the first fixed size of the first information blocks as data received from the trace buffer 227 (representing the first information block) is formatted to include time stamp information and stored in FIFO (Edwards: Col. 7, Lines 27-31; Fig.2, Element 202) and compression being performed on the PC (Edwards: Fig 11A & 11B) which *obviously* changes the size of the information block. FIFO is storage sequential storage element re-presenting second information block, which differ in size from trace data information.

Edwards teaches outputting a sequence of the second information blocks *from the data processor integrated circuit (Fig.2 element 102)* via a plurality of terminals at a

transmission clock rate, which may be different from the processor clock rate as obvious from the rate converter teaching of Edwards (Edwards: Col.2 Lines 37-40, 40-58), said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks.

Applicant has presented arguments (Remarks: Pg. 19) that block size of the information in the trace buffer 227 is the same as FIFO 202 & trace port registers 212. Examiner respectfully disagrees, as Edwards explicitly teaches change in first fixed size as present in the trace buffer 227 by addition of information size (timestamp & address by the trace processor 205 & reference counter 217; Col.19 Lines 64-67; Col.20 Lines 1-7) and further teaches compression of the PC and other information (Edwards: Fig 11A &11B; Col.19 Lines 3-19). Further, Table 7(sic) 8 (Col.20) clearly shows the reference message sent out having 14 bytes content, which is different in size from the message size present the trace buffer 227 (8 bytes to max 24 bytes). Therefore Edwards explicitly teaches fist fixed size, second fixed size.

Arguendo even if Edwards does not teach the amended limitation, where "plurality of *first information blocks organized in a sequence*, each of said first information blocks having a first fixed size, wherein *a first number of consecutive ones of said first information blocks defines a sequence of consecutive bits of said emulation information, and wherein each of said first number of consecutive first information blocks defines part of said sequence of consecutive bits*; and receiving the plurality

of first information blocks and arranging the emulation information contained therein into a plurality of *second information blocks organized in a sequence*, each of said second information blocks having a second fixed size which differs from the first fixed size of the first information blocks, wherein a second number of consecutive ones of said second information blocks defines said sequence of consecutive bits, wherein each of said second number of consecutive second information blocks defines part of said sequence of consecutive bits, *and wherein said second number differs from said first number*..."

Baird teaches first information blocks organized in a sequence as coming in the debug queue in a FIFO memory (First in First out) (Baird: Col.3 Lines 37-44) having a consecutive number of first information blocks indicated by timestamp (Baird: Col.3 Lines 53-56) which defines the consecutive bits of emulation information sent to the external system. The first fixed size could be 16, 32 or 64 bits dictated by level of detail needed to be captured (Baird: Col.5 Lines 59-Col.6 Lines 3).
Further Baird teaches receiving plurality of first information blocks from the FIFO debug queue and second information blocks organized into sequence where the second fixed size is limited by number of pins going to external system (Baird: Col.10 Lines 41-53). The second fixed size, 16 bits differs from the first fixed size of 32 and 64 bits. The information is offloaded sequentially as the memory the debug information is held is FIFO (Baird: Col.3 Lines 37-44). Further Baird teaches, wherein *said second number differs from said first number*... (Baird: Col.11 Lines 5-43).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of one skilled in the art of "data rate transmission and manipulation" and Edwards to relate the processor rate and first fixed size to transmission rate and second fixed size as basic input output equation of any rate converter system taught by Edwards (Edwards: Col.2 Lines 37-40; *23-26*) which as Edwards teaches is necessary to maximize the use of the limited transmission bandwidth to external systems (Edwards: Col.2 Lines 40-58) with additional information added to first fixed size (e.g. timestamp, address).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of *Baird to Edwards* to offload the data from the chip in different packet size than it is captured in as the chip may not have the required bandwidth (output pins and transmission rate) to offload the data at capture rate and size (Baird: Col.2 Lines 38-45). Further motivation to combine is that Baird reference is cited on the Edwards patent and is analogous art in used to capture the trace data.

Regarding Claim 2

Edwards teaches second fixed size (Edwards: Col.20 Table 8 7(sic)) is smaller in size than the first fixed size (Edwards: Trace Buffer 227 Max 3*8bytes; Col. 17, Lines 45-52).

Regarding Claim 3

Edwards teaches that trace information present in the FIFO might contain other control information like timing, program counter and address data in a compressed format (Edwards: Col.18, Lines 44-49). An embodiment of compression code is also shown (Edwards: Col.19, Lines 20-59). This data is exported the debug tool on the external system (Edwards: Col.6, Lines 33-35) the tool reconstructs the message and control information (Edwards: Col.19, Lines 18-20).

Regarding Claim 4

Edwards teaches that first information block may be packets on a switched communication medium (Edwards: Col.5, Lines 43-46) and second information blocks are made from first information blocks and are inform of packets (Edwards: Col.8, Lines 58-60; Col.7, Lines 31-38) to be sent to an external system over a transmission circuit.

Regarding Claim 16 (Updated)

Apparatus of claim 16 performs and is directed at the same functionality as the method of claim 1 and is thus rejected in the like manner. A data processor in the claim 16 is equivalent to data processor in claim 1. A collector in claim 16 is performing the same step of the method as the collection process in the claim 1. An exporter in claim 16 (coupled to the collector) performs the function of receiving trace data (from collector) and re-arranging trace data, as in method-step of claim 1. An exporter coupled to plurality of terminals to output the data is performing the same function as "outputting in sequence" step in claim 1. Further claim 16 states that all these components are part of an integrated circuit. Edwards teaches that data processor, collector and exporter can be on the same integrated circuit (Edwards: Fig.1, Element 101). The added limitations are also addressed similarly as in claim 1 – please see Baird's teachings, which further buttresses the common knowledge in the art of trace collection and distribution.

Regarding Claim 17

Claim 17 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 27 (Updated)

System of claim 27 performs and is directed at the same functionality as the method of claim 1 and is thus rejected in the like manner. Edwards teaches that data processor (Edwards: Fig.1, Element 102), emulation controller (Edwards: Fig.1, Element 103-Debug unit), apparatus to convey emulation information between

processor and emulation controller (Edwards: Fig.2, Element 227 (trace buffer), 220(capture buffer), 206(trace data latch)) and exporter (Edwards: Fig.2, Element 215, 106) can be on the same integrated circuit (Edwards: Fig.1, Element 101). An exporter coupled to plurality of terminals to exporter the data is performing the same function as "outputting information" step in claim 1. The added limitations are also addressed similarly as in claim 1 – please see Baird's teachings, which further buttresses the common knowledge in the art of trace collection and distribution.

Regarding Claims 28 & 29

Teachings of Edwards are disclosed above in claims 27. Edwards also teaches that the debug system (emulation controller) is connected to external system (Edwards: Col.6, Lines 12-14). An external system could be a host computer running the debug tool mentioned by Edwards (Edwards: Col 7, Lines 46-48). A keyboard constitutes a "tactile interface" and a computer monitor constitutes a "visual interface". Official notice is taken that it is extremely well known in the art to use a keyboard and a computer monitor with a computer (host interface) to form a man-machine interface.

Regarding Claim 34

Claim 34 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 37 (Updated)

Edwards also teaches rate conversion system (Edwards: Col.2 Lines 36-40) making the transmission speed variable and adjustable. Further, Edwards teaches that trace system (transmission clock) operate independent to the internal clock speed of the

processor (Edwards: Col.2 Lines 23-27), whereby the transmission speed is design choice. Microsoft dictionary defines the communications controller & communications parameters as follows:

> Communications controller: A device used as an intermediately in transferring communications to and from the host computer to which it is connected. [...]. A communications controller can be either programmable machine in its own right or a non-programmable device designed to follow a certain communications protocols.
>
> Communications Parameters: Any of the several settings required in order to enable computers to communicate. In asynchronous communications, for example, modem speed *(transmission rate)*, number of data bits and stop bits, and type of parity are parameters that must be set correctly to establish communications between two modems.

It would be obvious to one skilled in the art of communications that the transmission rate conversion is a design choice known to the designer.

Baird also teaches performing said collecting at a data collection clock rate (processor rate), and performing said outputting at a transmission clock rate (Baird: Col.3 Lines 41-47).

Regarding Claim 38

As indicated the by Edwards the fixed size of the trace may be at the maximum of 3*64 bit in the trace buffer 227, i.e. trace buffer may occupy only one slot (8 bytes) (Edwards: Fig.8 Elements 808-810). Further, Edwards teaches trace messages (second fixed size) in byte increments, which are greater in size than 8 bytes (Edwards: Tables 4-8) thereby teaching second fixed size greater than first fixed size.

Regarding Claim 39 (Updated)

Edwards teaches transmission clock rate is less than data processor clock rate (Edwards: Col.8 Lines 30-45) where the clock frequency is divided and fed to the

trace processor, thereby reducing the effective transmission frequency. Further, Edwards also teaches rate conversion system (Edwards: Col.2 Lines 36-40) making the transmission speed variable and adjustable. *Baird also teaches performing said collecting at a data collection clock rate (processor rate), and performing said outputting at a transmission clock rate (Baird: Col.3 Lines 41-52).*

Regarding Claims 43-45 (Updated)

Claims 43-45 disclose similar limitations as claims 37-39 respectively and are rejected for the same reasons as claim 37-39 respectively. Baird also teaches performing said collecting at a data collection clock rate (processor rate), and performing said outputting at a transmission clock rate (Baird: Col.3 Lines 41-47).

Regarding Claims 49-51 (Updated)

Claims 49-51 disclose similar limitations as claims 37-39 respectively and are rejected for the same reasons as claim 37-39 respectively. Baird also teaches performing said collecting at a data collection clock rate (processor rate), and performing said outputting at a transmission clock rate (Baird: Col.3 Lines 41-47).

9. Claims 30,32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. US Patent No 6,732,307 issued to Edwards in view of U.S. Patent No. 5,848,264 issued to Baird et al, further in view of U.S. Patent No. 6,229,808 issued to Teich et al (Teich hereafter).

Regarding Claims 30

Teaching of Edwards relating to collection of trace information in first fixed size and second fixed size is provided in respective parent and/or independent claim rejection in previous office action. Edwards teaches current packet register as target port registers (Fig.2 Element 212).

Edwards does not teach the new limitations where the second fixed size information block "is" and "is not" in multiples of first information blocks explicitly. Further, Edwards also does not explicitly teach arranging and selecting the bits from the first fixed size and vise versa. Baird also teaches the first and second block size are multiple (Baird: Col.5 Lines 59-Col.6 Lines 3, Col.10 Lines 41-53).

Teich teaches a first fixed size (Teich: Fig.9 ATM Cells) is an integral multiple of second fixed size (Teich: Fig.9 Local Data Package). The selecting and arranging is obvious in the design as for conversion between ATM package and Local package (Teich: Fig.9; Col.5 Lines 50-Col.6Lines21) would necessitate the need for selecting bits.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of *Baird to Edwards* to offload the data from the chip in different packet size than it is captured in as the

chip may not have the required bandwidth (output pins and transmission rate) to offload the data at capture rate and size (Baird: Col.2 Lines 38-45). Further motivation to combine is that Baird reference is cited on the Edwards patent and is analogous art in used to capture the trace data.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of *Teich to Edwards* to convert the first fixed block of information into second fixed block of information. The motivation to combine would have been that Teich simplifies the design of packet switching by providing little or no translation of data while changing from one fixed size to another (Teich: Col.1 Lines 46-50).

Regarding Claim 32

Claim 32 disclose similar limitations as claims 30 respectively and are rejected for the same reasons as claim 30.

Regarding Claim 35

Claim 35 disclose similar limitations as claims 30 respectively and are rejected for the same reasons as claim 30.

10. Claims 31, 33 & 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. US Patent No 6,732,307 issued to Edwards in view of U.S. Patent No. 5,848,264 issued to Baird et al, further in view of U.S. Patent No. 5,953,339 issued to Baldwin al (Baldwin hereafter).

Regarding Claims 31

Teaching of Edwards relating to collection of trace information in first fixed size and second fixed size is provided in respective parent and/or independent claim rejection in previous office action. Edwards teaches current packet register as target port registers (Fig.2 Element 212).

Edwards does not teach the new limitations where the second fixed size information block "is" and "is not" in multiples of first information blocks explicitly. Further, Edwards also does not explicitly teach arranging and selecting the bits from the first fixed size and vise versa including the use of last and current packet register. Baird not also teach this limitation.

Baldwin teaches a first fixed size (Teich: Fig.1 LLC packets) is a forming a *non-integral multiple of second fixed size* (Teich: Fig.1 ATM packets). The selecting and arranging is obvious in the design as for conversion between ATM packets and LLC packets (Teich: Fig.9; Col.5 Lines 50-Col.6Lines21) would necessitate the need for selecting bits and remembering last LLC packet bits.

Motivation to combine Baird with Edwards is same as disclosed in claim 1.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Baldwin to Edwards. The

motivation to combine would have been that Baldwin teaches better compaction technique instead of bit stuffing technique used in alternate implementation when the inter-packet conversion sizes are non-integral multiples. The advantages of compaction and bit stuffing technique are well known in the art.

Regarding Claim 33

Claim 33 disclose similar limitations as claims 31 respectively and are rejected for the same reasons as claim 31.

Regarding Claim 36

Claim 36 disclose similar limitations as claims 31 respectively and are rejected for the same reasons as claim 31.

11. Claim 40-42, 46-48 & 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6,732,307 issued to Edwards, in view of U.S. Patent No. 5,848,264 issued to Baird et al, further in view of U.S. Patent No. 5,953,339 issued to Baldwin al (Baldwin hereafter), further in view of U.S. Patent No. 5,790,398 issued to Horie (Horie hereafter).

Regarding Claim 40-42

Teachings of Edwards Baird & Baldwin are shown in the claim 31 rejection above. Edwards teaches stalling of operation in case of inability to transmit (due to buffer overflow) (Edwards: Fig.2 Elements 219 and 202).

Edwards, Baird and Baldwin do not teach use of NOP bit if no first information block is available for transmission.

Horie teaches use of NOP bits as pseudo-transmission data transmission, indicating that no data is being transmitted and for synchronization purpose (Horie: Fig.3C; Col.6 Lines 25-34). It would be obvious to use the NOP when no data is present to be transmitted from the teachings of Horie and initializing the NOP bits in first information block.

Motivation to combine Baird with Edwards is same as disclosed in claim 31.

Motivation to combine Edwards with Baldwin is presented above claim 31 rejection above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Horie to Edwards & Baldwin. The motivation to combine would have been that Edwards teaches

synchronization when the references are not absolute values (Edwards: Col.20 Lines 7-33) and Horie teaches synchronization through the NOP operation to stop the performance from deteriorating (Horie: Col.2 Lines 3-14; Col.6 Lines 25-34).

Regarding Claims 46-48

Claims 46-48 disclose similar limitations as claims 40-42 respectively and are rejected for the same reasons as claim 40-42 respectively.

Regarding Claims 52-54

Claims 52-54 disclose similar limitations as claims 40-42 respectively and are rejected for the same reasons as claim 40-42 respectively.

Conclusion

1. All claims are rejected.
2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
3. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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